YFS1224

12bit ADC MTP MCU with 2K-bit EEPROM

Datasheet

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Table of content

Revision History

Revision	Date	Description
0.00	2025/07/10	Preliminary version

1. Description

YFS1224 series mainly consists of two parts：

- PFS122B MCU
- 2Kbit EEPROM

Among them, PFS122B is a 12bit ADC type MTP MCU, supporting Mini-C / ASM language, easy to program. For details on the use of PFS122B, please refer to the "PFS122B Datasheet" on PADAUK’s official website.

The built-in 2K-bit EEPROM, as an I²C-compatible serial EEPROM (electrically erasable programmable memory) device, contains a 256×8-bit memory array with 8 bytes per page, which can provide more data storage for the MCU Take space.

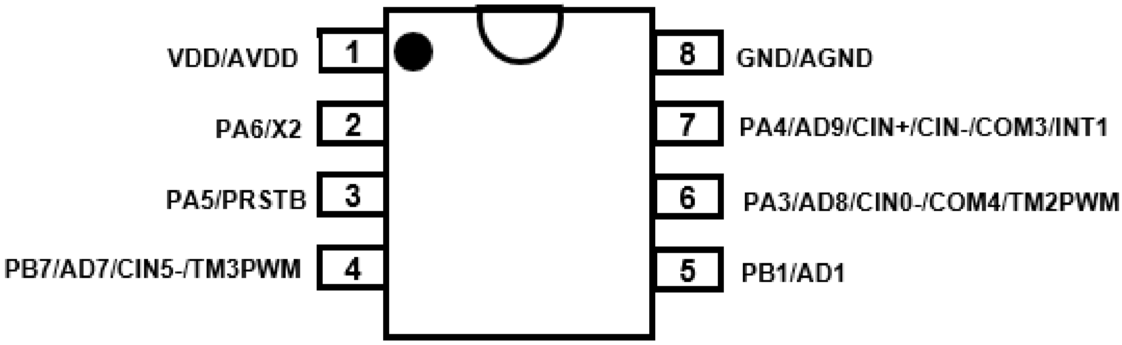
The main storage space of YFS1224 are as follows：

- MTP ROM（Word）：1.9K
- SRAM（Byte）：128
- EEPROM：2K bit = 256×8bits = 32 page × 8 bytes

2. Application

- toys
- home appliances
- LED lighting products
- General electronics

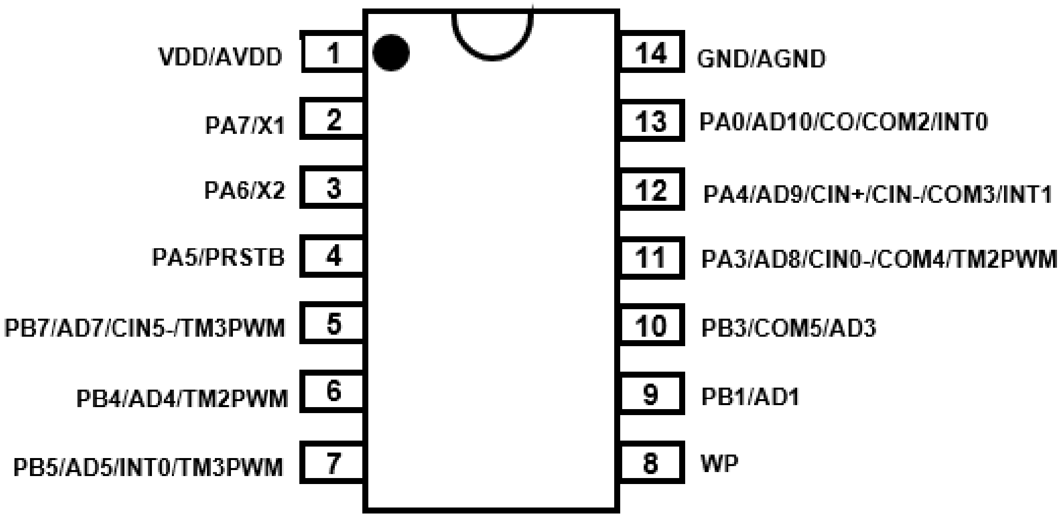
3. Ordering / Package Information



YFS1224-S08A (SOP8-150mil)

Note：

1. PB2 TO E^2_ SCL ， PB0 TO E^2_ SDA，PB6 TO E^2_ VDD;
2. MCU_GND,24C02_GND,24C02_WP common ground;



YFS1224-S14A (SOP14-150mil)

Note：

1. PB2 TO E^2_ SCL ， PB0 TO E^2_ SDA，PB6 TO E^2_ VDD；
2. MCU_GND,24C02_GND common ground;

Pin Name	Input / Output				Special features							
	I / O	Pull-high	Wake-up	open-drain output	Crystal	Comparator	PWM	External interrup	External Reset	EEPROM	Writing	ADC
PA0	√	√	√			CO	PG0	INT0				AD10
PA3	√	√	√			CIN-	TM2 PG2				√	AD8
PA4	√	√	√			CIN+ CIN-	PG1	INT1A			√	AD9
PA5	√	√	√	√					√		√	
PA6	√	√	√		Xout						√	
PA7	√	√	√		Xin							
PB0	√	√								SDA		
PB1	√	√	√									AD1
PB2	√	√								SCL		
PB3	√	√	√				PG2					AD3
PB4	√	√	√				TM2 PG0					AD4
PB5	√	√	√				PG0 TM3	INT0A				AD5
PB6										EVDD*		
PB7	√	√	√			CIN-	TM3 PG1					AD7
WP										√		
VDD/ AVDD											√	
GND/ AGND										EGND	√	
Note	1. VDD/AVDD: VDD is the MCU digital positive power supply, AVDD is the ADC dedicated analog positive power supply. Inside the MCU, AVDD and VDD are connected together (double bonding), while externally they are the same pins. 2. GND/AGND: GND is the MCU digital ground pin, AGND is the ADC analog ground pin. Inside the MCU, AGND and GND are connected together (double bonding), while outside the same pin. 3. EVDD/EGND: EEPROM power supply pin; S08, S14 package EVDD powered by PB6, when using E2, please make sure to output PB6 high in the program. 4. The address lines A0, A1, and A2 of the EEPROM are pulled down to EGND by default.											

	5. PB0 and PB2 are the normal I/O ports of the PFS122B, but are dedicated to communicating with the EEPROM internally, and are not available for other external uses. 6. WP is the write-protect input of EEPROM, used for hardware data protection. When it is connected to a low level, the EEPROM can be read/written normally, and when it is high, the EEPROM can only be read but not written; this pin is only open in the S14 package, and the S08 has been connected to GND internally.

4. EEPROM Device Characteristics

4.1. Reliability Parameters [1]

Symbol	Description	Min	Typ	Max	Unit
EDR [2]	Endurance	1,000,000			Write Cycle Time
DRET	Data retention	100			year

Notes：

[1] This parameter is determined by characterization and is not 100% tested

[2] Conditions：25℃，3.3V，page mode.

4.2. Capacitance [1]

Symbol	Description	Max	Unit	Conditions
$C_{I/O}$	Input / Output Capacitance (SDA)	8	pF	$V_{I/O}$=GND
C_{IN}	Input Capacitance (E0, E1, E2, WCB, SCL)	6	pF	V_{IN}=GND

Notes： [1] Conditions：T_A = 25 ℃, F = 1MHz, V_{CC} = 5.0V.

4.3. DC Description

Unless IMPORTANT NOTICE, the following data are measured at V_{CC} = 1.7V ~ 5.5V, T_A = -40 ℃ ~ 85 ℃

Symbol	Description	Min	Typ	Max	Unit	Conditions
$E2V_{CC}$	DC supply voltage	1.7		5.5	V	
I_{sb}	Standby Current	-	-	1.0	uA	V_{CC} = 3.3V, T_A = 85℃
		-	-	3.0	uA	V_{CC} = 3.3V, T_A = 85℃
I_{CC1}	Supply Current	-	0.2	0.4	mA	V_{CC}=5.5V, read@400Khz
I_{CC2}	Supply Current	-	0.8	1.6	mA	V_{CC}=5.5V, write@400Khz
I_{LI}	Input Leakage Current	-	0.1	1.0	uA	V_{IN} = V_{CC} or GND
I_{LO}	Output Leakage Current	-	0.05	1.0	uA	V_{OUT} = V_{CC} or GND
V_{IL}	Input Low Level	-0.6	-	0.3V_{CC}	V	
V_{IH}	Input High Level	0.7V_{CC}	-	V_{CC}+0.5	V	
V_{OL1}	Output Low Level V_{CC}= 1.7V (SDA)	-	-	0.2	V	I_{OL} = 1.5 mA
V_{OL2}	Output Low Level V_{CC}= 3.0V (SDA)	-	-	0.4	V	I_{OL} = 2.1 mA

4.4. AC characteristic

Unless IMPORTANT NOTICE, the following data are measured under V_{CC}= 1.7V ~ 5.5V, T_A = -40 ℃ ~ 85℃ , C_L=100pF, and the test conditions are in Notes [2].

Symbol	Description	1.7≤V_{CC}<2.5			2.5≤V_{CC}≤5.5			Unit
		Min	Typ	Max	Min	Typ	Max	
f_{SCL}	Clock Frequency, SCL	-	-	400	-	-	1000	KHz
t_{LOW}	Clock Pulse Width Low	1.3	-	-	0.4	-	-	us
t_{HIGH}	Clock Pulse Width High	0.6	-	-	0.4	-	-	us

Symbol	Description	$1.7 \le V_{CC} < 2.5$			$2.5 \le V_{CC} \le 5.5$			Unit
		Min	Typ	Max	Min	Typ	Max	
t_{AA}	Clock Low to Data Out Valid	0.05	-	0.9	0.05	-	0.55	us
t_{I}	Noise Suppression Time	-	-	0.1	-	-	0.05	us
t_{BUF}	Time the bus must be free before a new transmission can start	1.3	-	-	0.5	-	-	us
$t_{HD.STA}$	Start Hold Time	0.6	-	-	0.25	-	-	Us
$t_{SU.STA}$	Start Setup Time	0.6	-	-	0.25	-	-	us
$t_{HD.DAT}$	Data In Hold Time	0	-	-	0	-	-	us
$t_{SU.DAT}$	Data In Setup Time	0.1	-	-	0.1	-	-	us
t_{R}	Inputs Rise Time[1]	-	-	0.3	-	-	0.3	us
t_{F}	Inputs Fall Time[1]	-	-	0.3	-	-	0.1	us
$t_{SU.STO}$	Stop Setup Time	0.6	-	-	0.25	-	-	us
t_{DH}	Data Out Hold Time	0.05	-	-	0.05	-	-	us
t_{WR}	Write Cycle Time	-	-	5	-	-	5	ms

Notes： [1] This parameter is determined by characterization and is not 100% tested.

[2] AC measurement conditions:

- ✧ R_L (connected to V_{CC})：1.3k (2.5V, 5.5V), 10k (1.7V)
- ✧ Input pulse voltage：$0.3V_{CC} \sim 0.7V_{CC}$
- ✧ Input rise/fall time：≤50ns
- ✧ Input/output timing reference voltage：$0.5V_{CC}$

5. Internal communications

5.1. Bus Timing

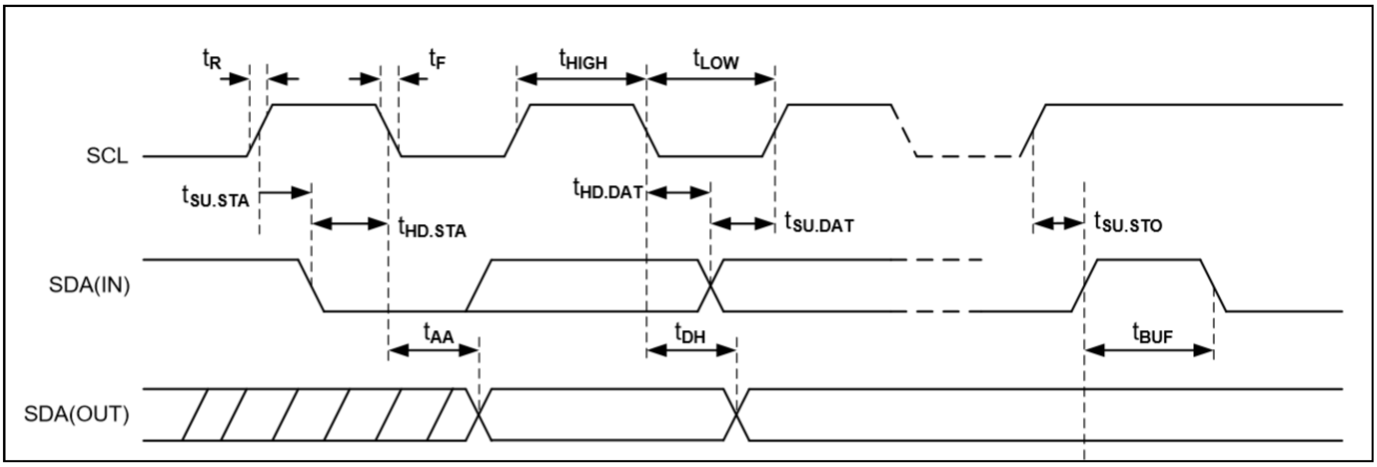


Fig 1: Bus Timing Diagram

5.2. Write cycle timing

The write cycle time, t_{WR}, is the time from the valid end signal of a write sequence to the end of the internal clear/write cycle.

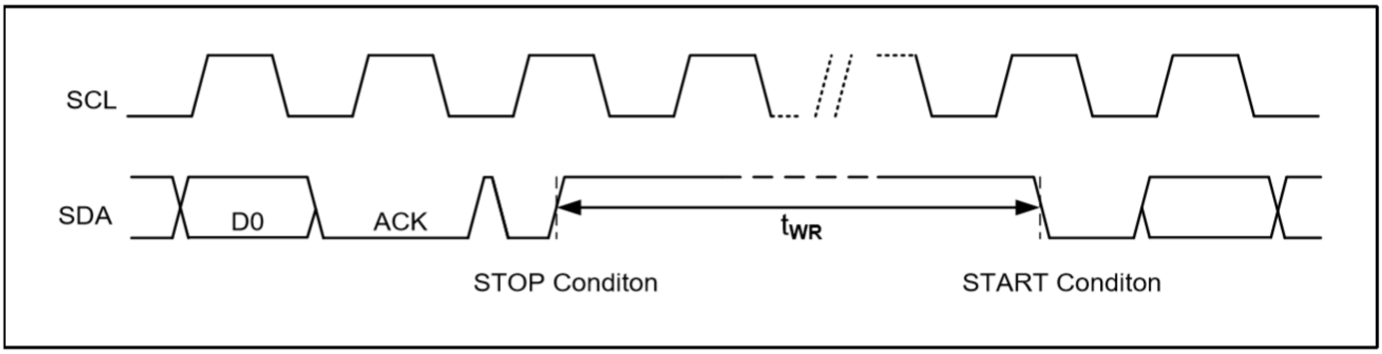


Fig 2: Write cycle timing diagram

5.3. EEPROM communication signal

The communication signal line between EEPROM and MCU is as follows:

EEPROM_SDA <==> MCU_PB7，EEPROM_SCL <==> MCU_PB0

Data changes on the SDA pins can only be done with SCL low, and SDA changes during SCL high will represent start and end signals.。

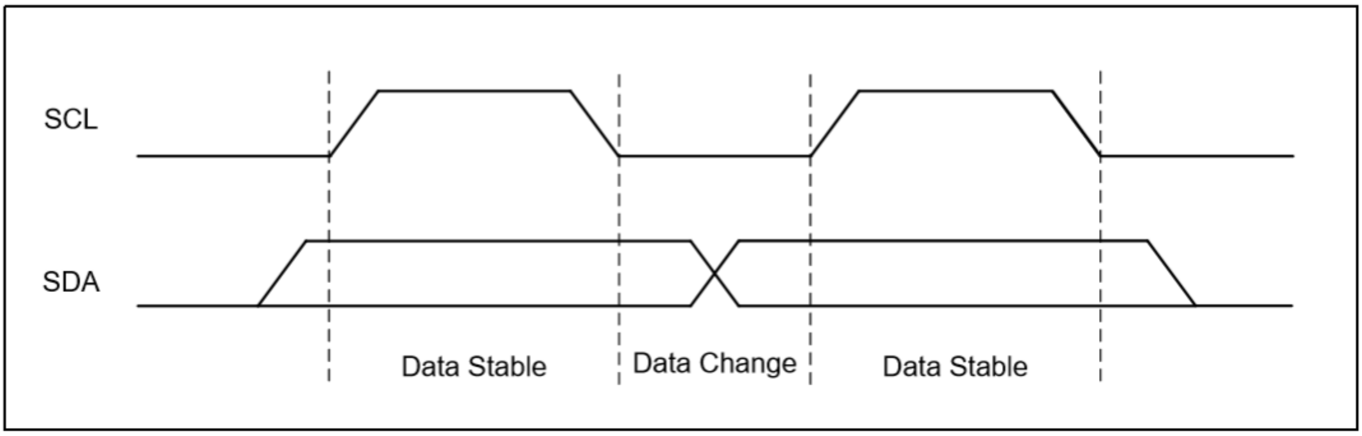


Fig 3：Data Validity

5.3.1. Start and stop signals（Start / Stop）

With SCL high, a change in the rising or falling edge of the data line SDA will indicate the beginning or end of the data transfer as shown below:

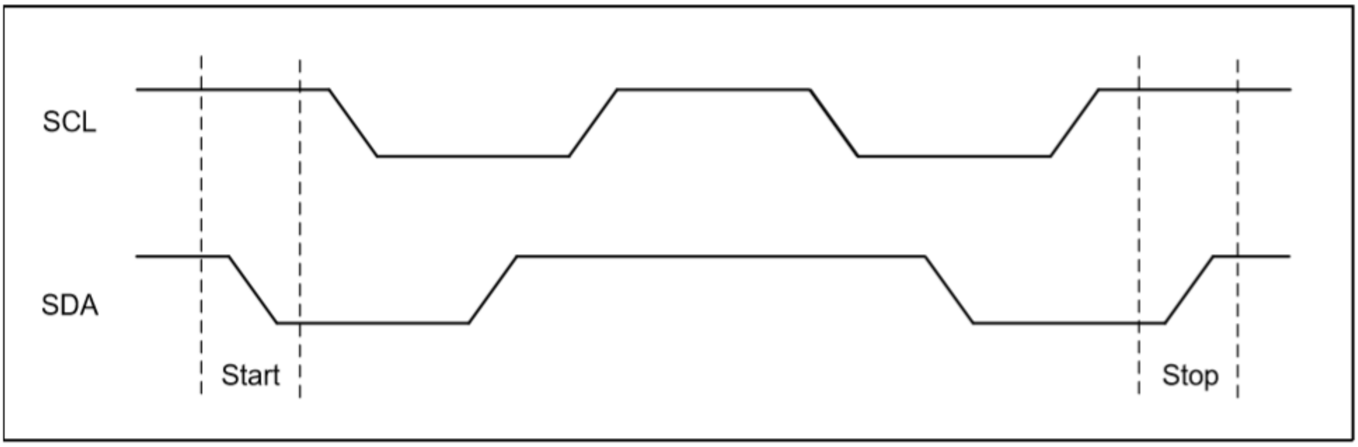


Fig 4: Start and stop signals

5.3.2. Response Signal（ACK）

After each byte (8 binary bits) is received, at the ninth clock signal, the EEPROM will respond with a low-level ACK response signal on SDA to indicate that the current device has received a byte. The transmission of the next byte can begin. The timing diagram is as follows:

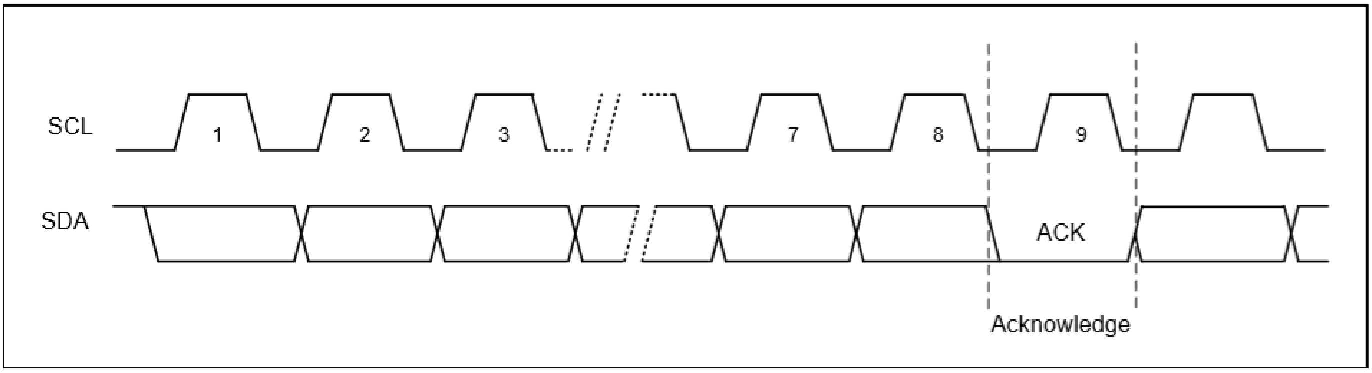


Fig.5：Response signal

5.3.3. Standby mode

The built-in EEPROM of YYFS1224 has a low-power standby mode, which can be enabled by the following conditions：

a. After powering connected；

b. Receive end signal in read mode；

c. After completing all internal operations.

5.3.4. Software Reset

After protocol interruption, power off or system reset, the EEPROM can be reset through the following steps：

a. Create a start signal；

b. Enter 9 clocks continuously；

c. Create another start signal followed by an end signal。

After completing the above steps, the EEPROM can perform the next communication, as shown in the figure below.

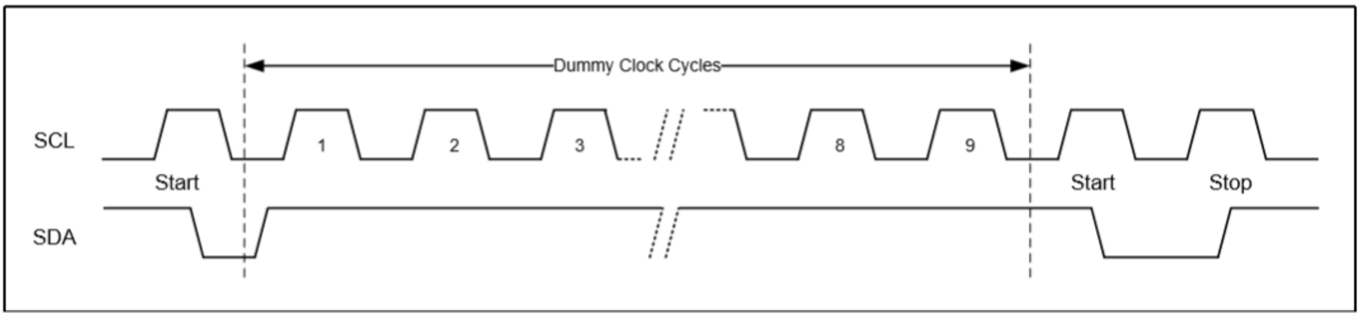


Fig.6：Software reset signal

5.4. EEPROM communication signal

5.4.1. Device address

In the YFS1224 series, the device address of EEPROM is 0B1010_000_x. Among them, the numbers of Bit7 - Bit1 are fixed, and the lowest bit Bit0 is used as the read and write operation bit R/W, which can be 0 or 1. When the R/W bit is 0, the device performs a write operation by default; conversely, when the R/W bit is 1, the device performs a read operation by default.

The EEPROM will compare the address code in the read/write operation command with the actual address of the device 0B1010_000_x. If the compared device addresses are consistent, the device will output a "0" to respond. Otherwise, the device will return to standby state.

Bit 7 （MSB）	Bit 6	Bit 5	Bit 4	Bit 3 （E2）	Bit 2 （E1）	Bit 1 （E0）	Bit 0 （LSB）
1	0	1	0	0	0	0	R/W

5.4.2. Data Address

Bit 7 （MSB）	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 （LSB）
A7	A6	A5	A4	A3	A2	A1	A0

5.4.3. Single Byte Write Operation

The write single-byte instruction can only write one byte of data to an address in the chip at a time.

First, a start signal is sent to notify the chip to start command transmission, and then the set device address is transmitted. At this time, the R/W bit should be set to 0, followed by the eight-bit data address, and then the eight-bit data word to be written. Finally, the end signal is sent to indicate the end of this instruction.

The EEPROM returns an answer signal ACK to the MCU after receiving the device address, data address and data word.

After receiving the end command, the EEPROM will enter an internally timed write cycle in which all inputs are disabled and the EEPROM will not respond until the write is completed.

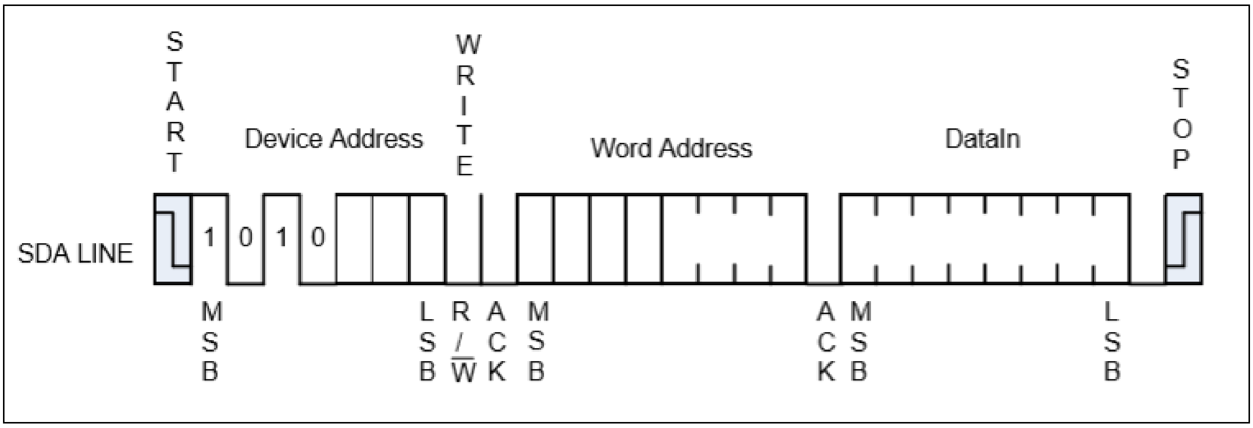


Fig.7：Single byte write timing diagram

5.4.4. Page Write Operation

The initialization of page write is the same as that of byte write, but the MCU will not send a stop condition after the first data word is locked. Instead, after the EEPROM acknowledges receipt of the first data word, the MCU can transmit more data words. The EEPROM will respond with a "0" after receiving each data word. After the page write data is written, the stop condition must be used to terminate the page write operation.

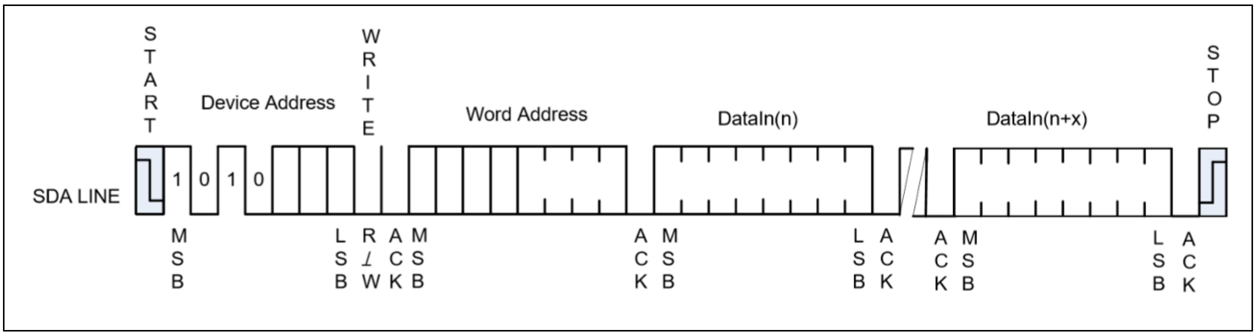


Fig.8：Page write timing diagram

The lower three bits of the data word address are internally incremented after each data word is received. The higher data word address bits are not incremented and the memory page row location is retained. When the internally generated data address reaches a page boundary, the subsequent data bytes to be written are rewritten at the beginning of the same page.

If more than 8 data words are transferred to the EEPROM, the data word address will be flipped and the previous data will be overwritten. Address rollover during a write is from the last byte of the current page to the first byte of the same page.

5.4.5. Answer Polling

Once the internally timed write cycle is started, the EEPROM will disable all inputs. At this time, the MCU can use acknowledgment polling to determine whether the EEPROM internal write is complete. Acknowledging a poll operation involves sending a start condition followed by the device address word. The R/W bit represents the desired read/write operation. Only when the internal write cycle is completed will the EEPROM respond with a "0", allowing the read/write operation to continue.

5.4.6. Read operation

Read operations are initiated in the same manner as write operations, except that the Read/Write select bit (R/W) in the device address word should be set to '1'. There are three types of read operations: current address read, random address read and sequential read, which are introduced separately below.

5.4.7. Read current address

The EEPROM internal address counter maintains the last address accessed during the last read or write operation and increments it by one. This address will remain valid between operations as long as the chip remains powered.

When the MCU sends the device address with the R/W bit set to "1" and receives a response from the EEPROM, the data word of the current address will be sent out with the clock. After receiving the data transmitted by the EEPROM, the MCU does not need to send a low-level ACK to the EEPROM. It can directly pull SDA high and wait for one clock before sending the end signal.

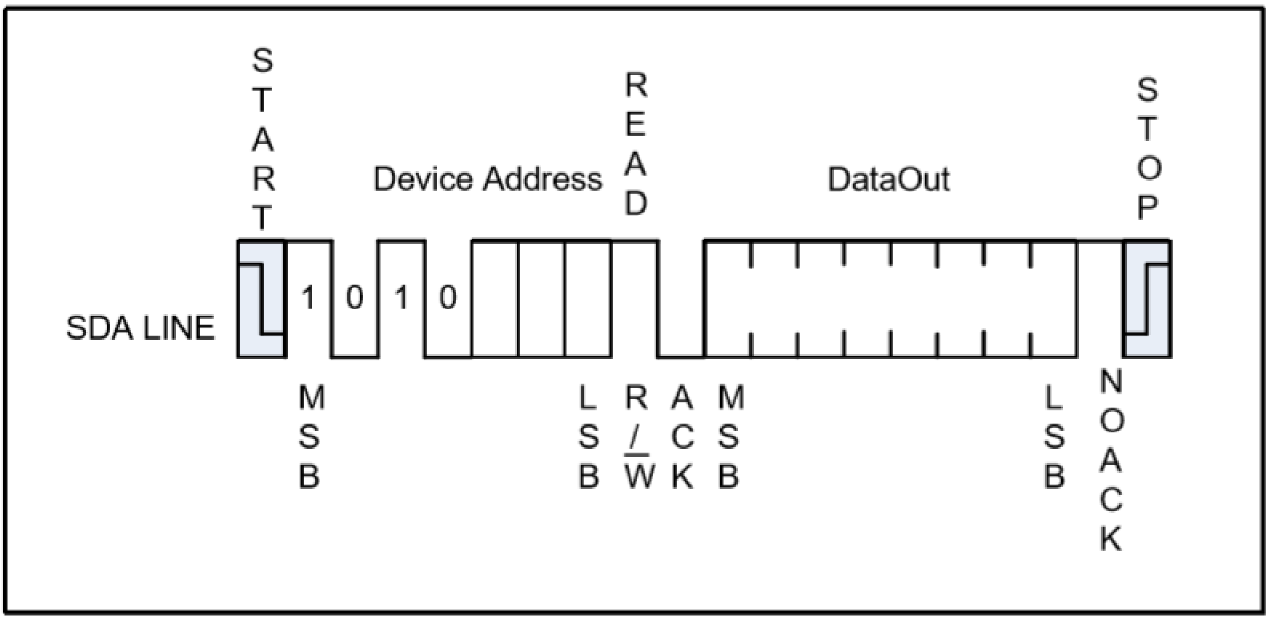


Fig.9：Read current address timing diagram

5.4.8. Random Read

Random reads require a "pseudo" byte write operation to load the data word address. Once the EEPROM receives the device address and data address and acknowledges the ACK, the MCU must give another start condition and then send a device address with R/W high to initiate the read operation.

EEPROM identifies the device address, and after responding to ACK, it continuously sends data words with the clock.

The MCU does not respond to "0", but generates an end condition, as shown in Figure 10

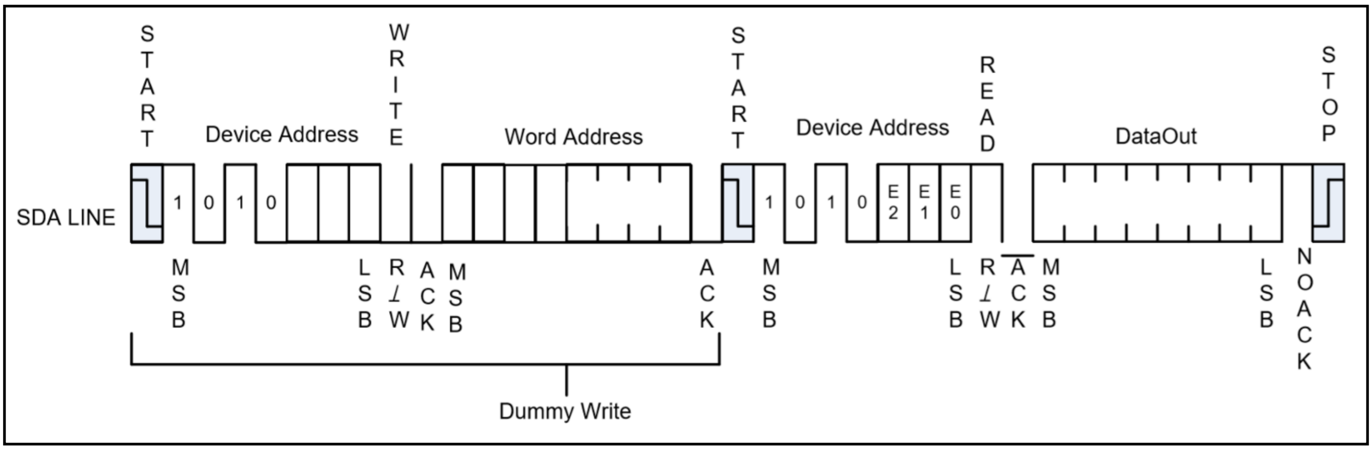


图 10：随机读取时序图

5.4.9. Sequential Reading

A sequential read is initiated by the currently read address or a random read address.

After receiving a data word, the MCU will respond with ACK. As long as the EEPROM receives an ACK, it continues to increment the data word address and output sequential data words continuously.

When the memory address limit is reached, the data word address is rolled over and sequential reading continues. Address rollover during a read is from the last byte of the last memory page to the first byte of the first page.

The sequential read operation will terminate when the MCU does not respond with "0" but generates an end condition, as shown in Figure 11.

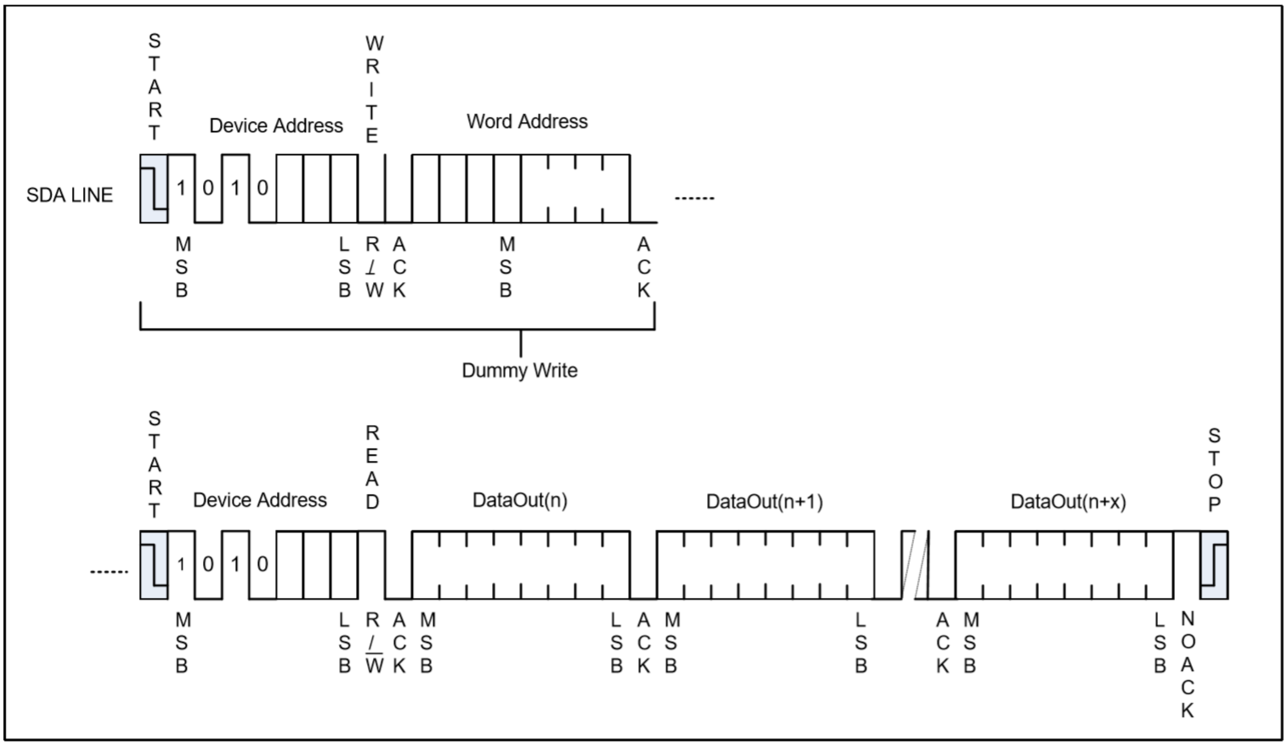


Fig.11：Sequential Read Timing

6. Programming

YFS1224 has a total of 5 programming pins, which are：VDD，PA3，PA5(VPP)，PA6，GND。

YFS1224 can only be programmed with **5S-P-003 and above versions of the writer.** And must specify the package specification in the code project “extern.h” file, the instruction is as follows: (The software environment defaults to S14 package, the IC using S14 package specification does not need to use this instruction. Note: This instruction can be used only after **IDE_0.99C3.**)

When using the YFS1224-S08A: **package => 'S08'**

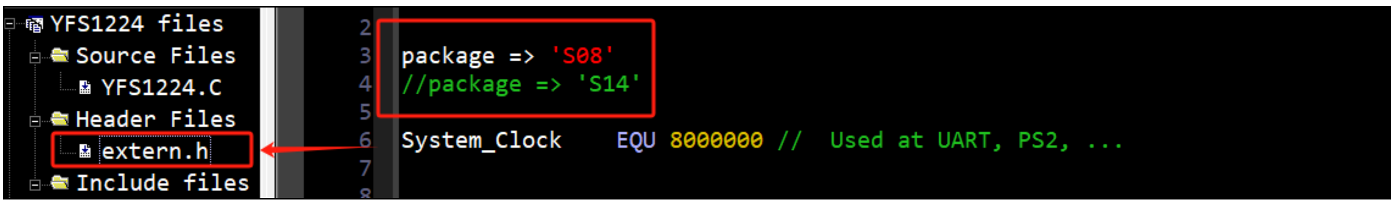


Fig 12: Example of Specify Package Specification Instruction

In addition: When programming the S14 package, simply insert the JP2 jumper cap for P003, and place the IC on the front side with 4 empty spaces.

When programming the S08 package, users need to make a programming signal adapter board by themselves through wire - jumping (the wire - jumping method is shown in Figure 13 below). Insert it into the JP7 position on the back of the writer, and check whether there are black jumper caps on other JPx pin headers. If so, please remove them. Users can also refer to the 5S-P-003 user manual to learn more about the manufacturing method of the JP7 programming signal adapter board. Place the IC at the top - most position on the front side of the writer.

Finally, the PIN1 of the chip is the top - left first pin on the textool. Program the chip when the writer shows "IC ready".

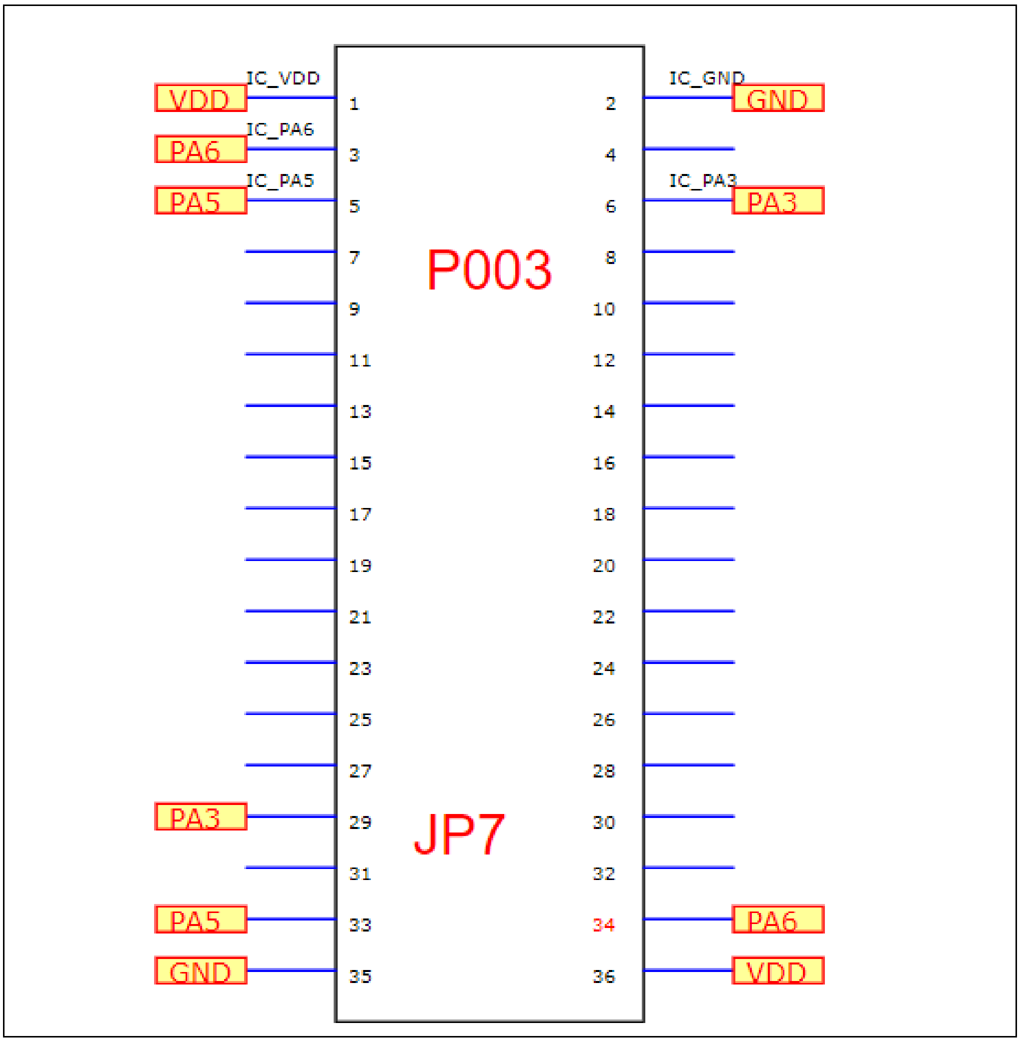


Fig 13：YFS1224-JP7 Diagram

7. Typical Application

Figure14 is one of the typical applications of the YFS1224 series, which is for user reference only.

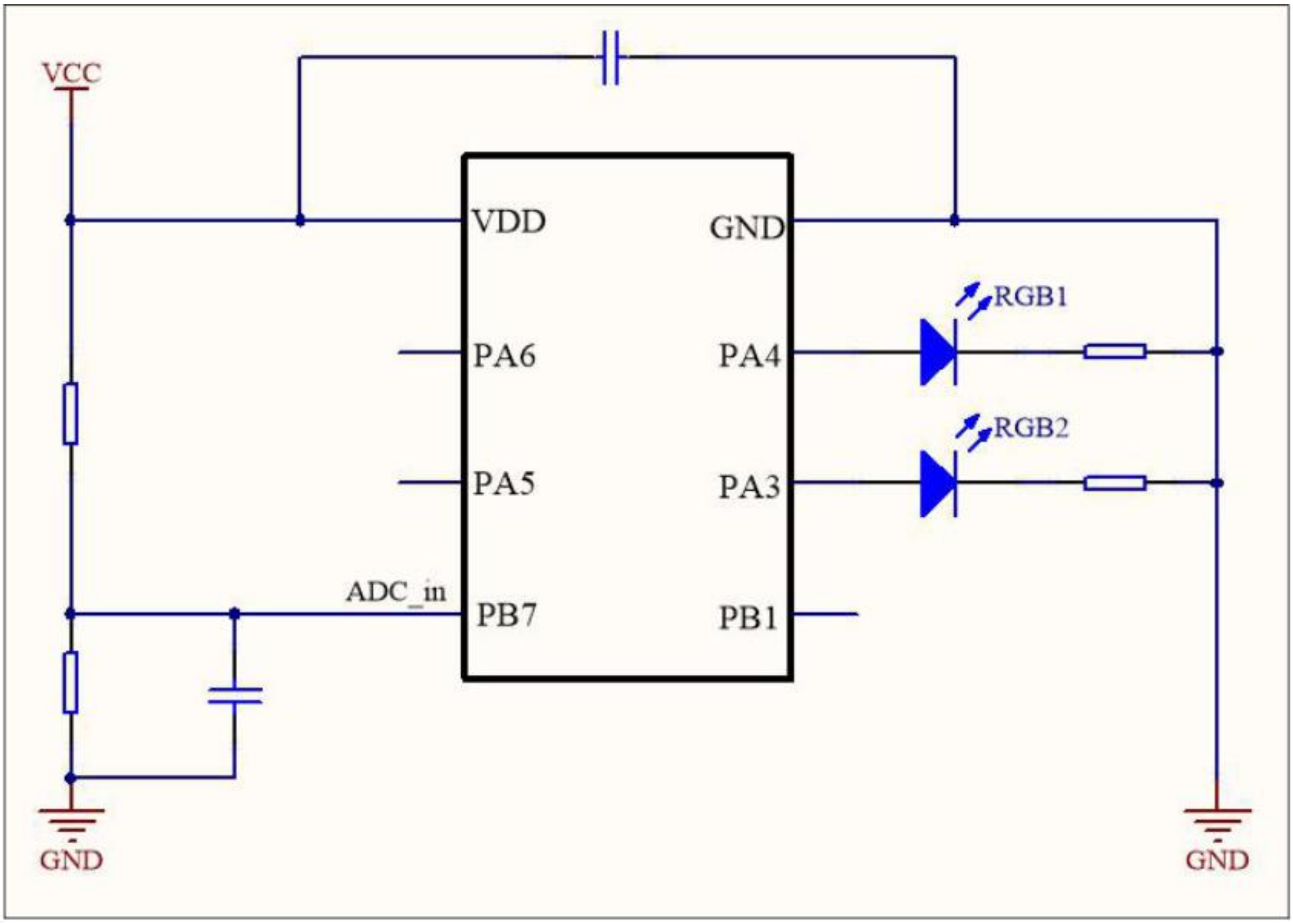


Fig 14：YFS1224 typical application schematic.

8. Project file Demo

The Demo contains the program framework of YFS1224 and the example of E2; please contact our FAE for the engineering documents.

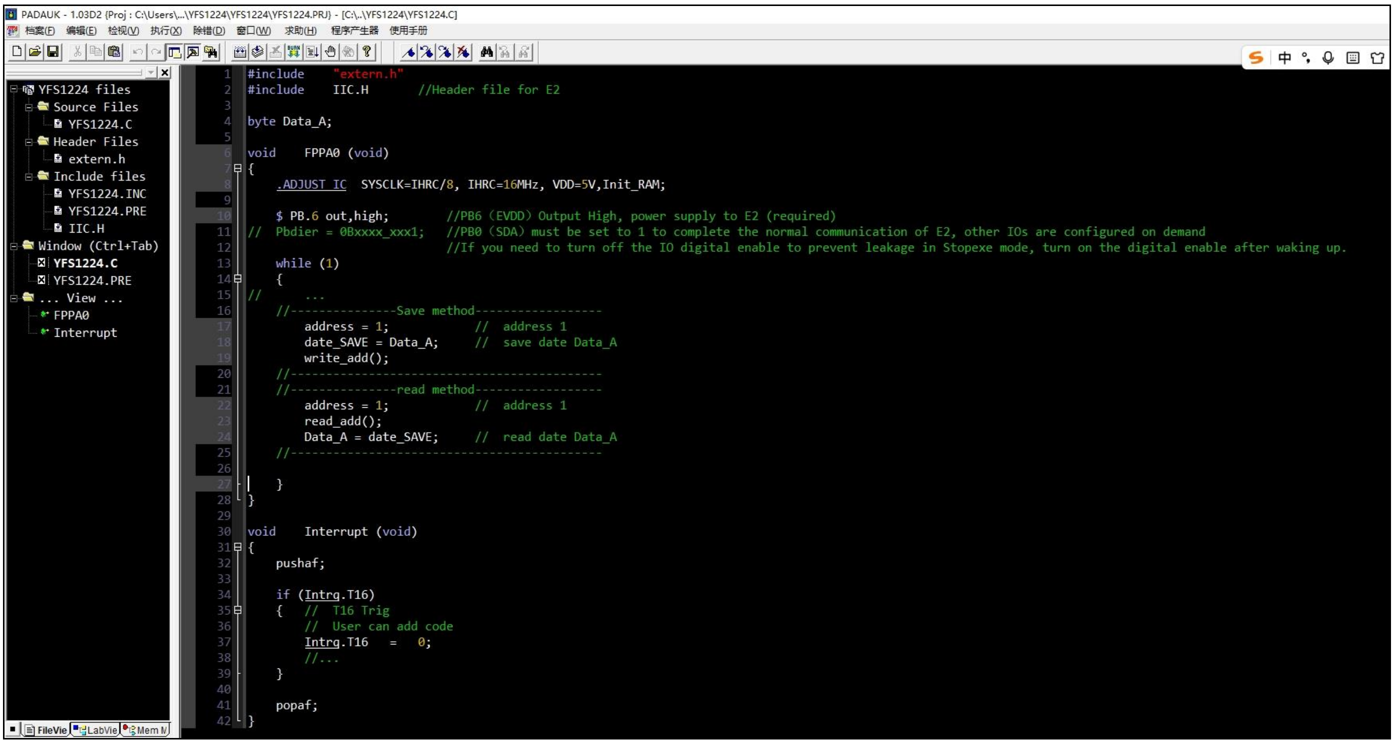
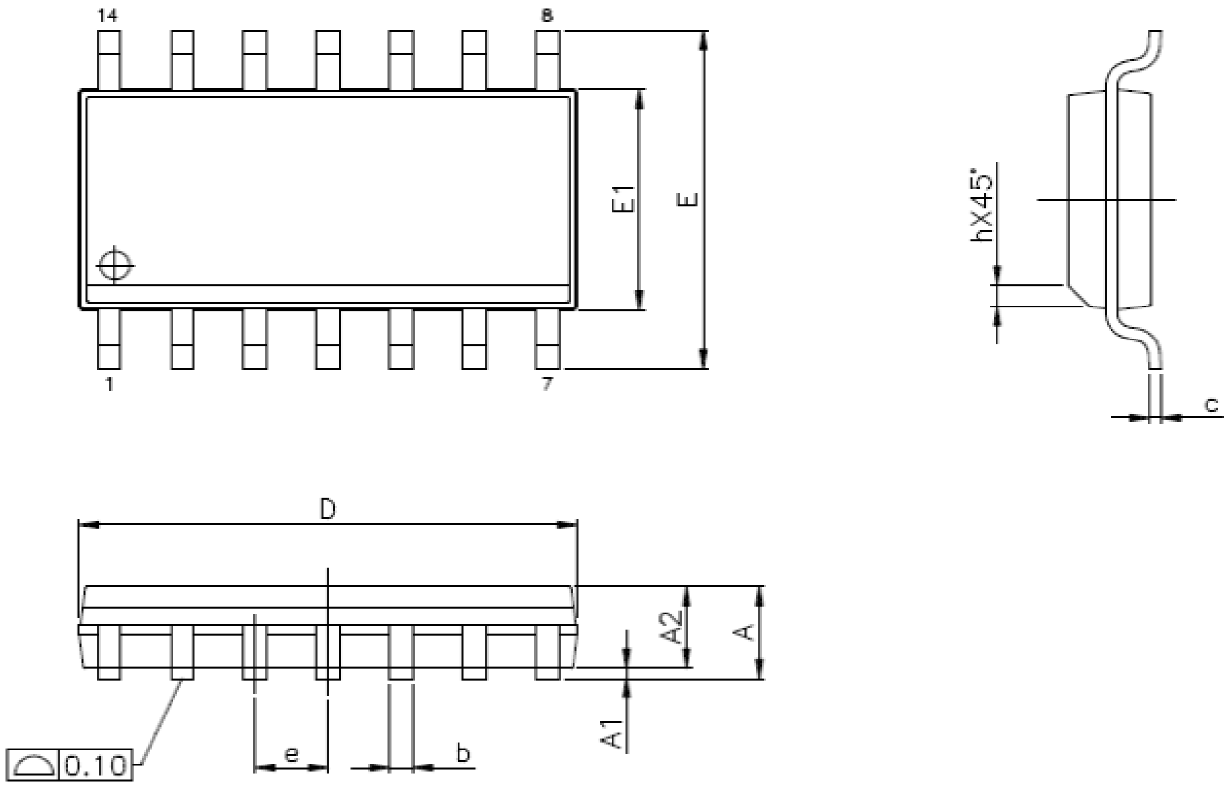


Fig 15: Project file Demo file display

9. Package Information

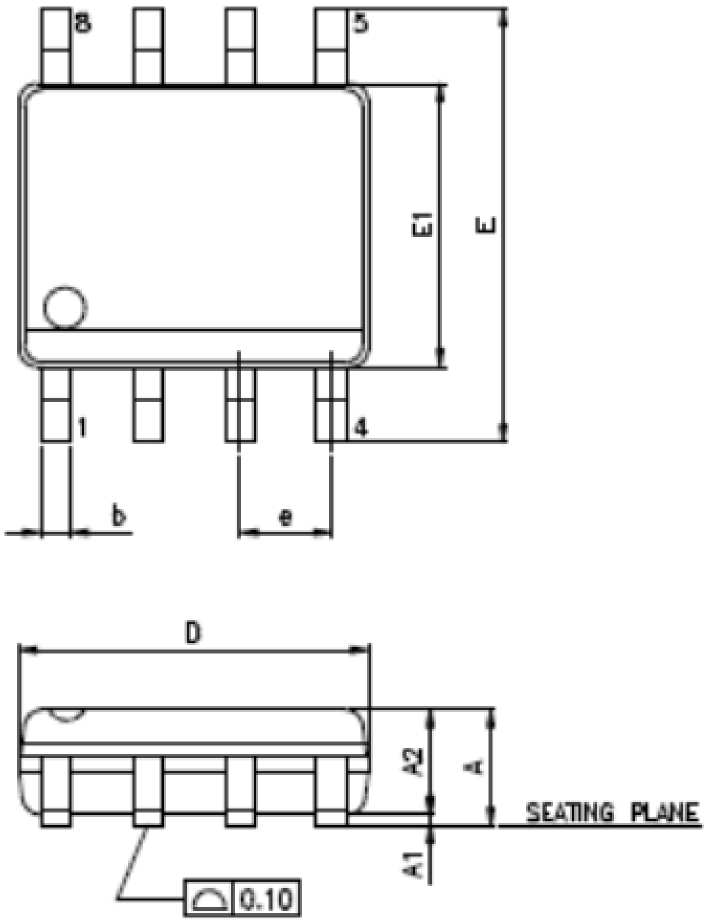
YFS1224 is available in SOP14 and SOP8 packages, the specific size parameters are as follows:

SOP14(Pitch=1.27mm=0.05inch, Body Width=3.9mm=150mil=0.15inch)



	MILLIMETERS	
SYMBOLS	MIN	MAX
A	-	1.75
A1	0.10	0.25
A2	1.25	-
b	0.31	0.51
c	0.10	0.25
D	8.65 BSC	
E	6.00 BSC	
E1	3.90 BSC	
e	1.27 BSC	
L	0.40	1.27
h	0.25	0.50
θ °	0	8

SOP8(Pitch=1.27mm=0.05inch, Body Width=3.9mm=150mil=0.15inch)



	MILLIMETERS	
SYMBOLS	MIN	MAX
A	-	1.75
A1	0.10	0.25
A2	1.25	-
b	0.31	0.51
c	0.10	0.25
D	4.90 BSC	
E	6.00 BSC	
E1	3.90 BSC	
e	1.27 BSC	
L	0.40	1.27
h	0.25	0.50
θ °	0	8